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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,207	KO ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,11,13-18,27,29,30,35-41,48,49 and 54-57* is/are rejected.

7)☒ Claim(s) *8,10,12,19-26,28,31-34,42-47 and 50-53* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/3/03&10/2/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 13 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 is misdescriptive to recite "each of said register including a plurality of data latch structures". However, the drawing shows that each of the data latch is a single register (see figures 6 and 7).

Claim 14 is rejected as including the indefinites of claim 13.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5, 9 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Ooishi et al. (USP 6621306).

As to claim 1, Ooishi et al. discloses in figure 3 a data latch apparatus, comprising: a first latch (44-49) for latching a data signal (D); a second latch (65-68) coupled to the first latch for

retaining the data signal while the first latch is inoperative (sleep mode); a save device (63, 64 and circuit, shown in figure 7, that provide signal ES) connected between the first and second latches for transferring the data signal from the first latch to the second latch, the save device including a first transistor (63) having a gate; and the first latch including a first node (/A) for providing the data signal to the save device, the gate connected to the first node.

As to claim 2, figure 3 shows that the first latch has a second node (A) for providing the data signal, the save device including a second transistor (64) having a gate connected to the second node.

As to claim 3, figure 3 shows that the first and second transistors are connected at a common node (ES) other than the first and second nodes.

As to claim 4, figure 7 shows that the save device includes a third transistor (75) connected to the common node.

As to claim 5, figure 7 shows that the third transistor has a gate for receiving a control signal (/SLP) which indicates when to transfer the data signal from the first latch to the second latch.

As to claim 9, figure 3 shows that the first latch includes an inverter (46-49) having an input and an output, and wherein the first node is the inverter input and the second node is the inverter output.

As to claim 11, figure 3 shows the second latch is for retaining the data signal while the first latch is inoperative due to removal of power therefrom.

5. Claims 17, 18, 27, 29, 30, 35, 41, 48 and 49 are rejected under 35 U.S.C. 102(e) as being anticipated by Zyuban et al. (US 20030188241).

As to claim 17, Zyuban et al.'s figure 6B shows a data latch apparatus, comprising: a first latch (the most left latch) for latching a data signal (I); a second latch (latch circuit in 60) coupled to the first latch for retaining the data signal while the first latch is inoperative; a restore device (the inverters in 60 that receive signal B and N1-N8) connected between the first and second latches, the restore device having an input for receiving a restore signal (RSTR, RSTR_B), the restore device responsive to the restore signal for transferring the data signal from the second latch to the first latch; and the restore device further for isolating the second latch from the first latch independently of the restore signal while the first latch is inoperative.

As to claims 18 and 41, figure 6B shows that the second latch has a first node (SCAN_OUT) for providing the data signal to the restore device, the restore device including a first transistor (N7) having a gate connected to the first node.

As to claims 27 and 49, figure 6B shows that the second latch has a second node (SCAN_OUT_B) for providing said data signal to the restore device, the restore device including a second transistor (N3) having a gate connected to the second node.

As to claim 29, figure 6B shows that the restore device includes a third transistor (N8) connected in series with the first transistor, the third transistor having a gate connected to the input.

As to claim 30, figure 6B shows that the restore device includes a fourth (N4) transistor connected in series with the second transistor, the fourth transistor having a gate connected to the input

As to claims 35 and 48, figure 6B shows that the second latch is for retaining the data signal while the first latch is inoperative due to removal of power therefrom.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 6, 7, 9, 11 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sani et al. (US 2003/0218231) in view of Coughlin, Jr. et al. (USP 6493257).

As to claim 1, Sani et al.'s figure 2 shows a data latch apparatus, comprising: a first latch ((220, 230) or (205, 260)) for latching a data signal. Sani et al.'s figure 2 fails to show "a second latch coupled to the first latch for retaining the data signal while the first latch is inoperative". However, Coughlin, Jr. et al.'s figure 1 shows a latch circuit (14 and 16) coupled to circuit 12, wherein circuit 12 can be any type of circuit, column 2, lines 54-57, for saving data of circuit 12 when circuit 12 is in a sleep mode. Therefore, it would have been obvious to one having ordinary skill in the art to add Coughlin, Jr. et al.'s latch circuit to at least one of Sani et al.'s latches for the purpose of saving the data in the first latch when it is in a sleep mode or inoperative. Thus, the modified Sani et al.'s figure 1 further shows a second latch (Coughlin, Jr. et al.'s T12-T14) coupled to the first latch for retaining the data signal while the first latch is inoperative; a save device (Coughlin, Jr. et al.'s T8-T11) connected between the first and second latches for transferring the data signal from the first latch to the second latch, the save device including a first transistor (T9) having a gate; and the first latch including a first node (node between 244 and 250) for providing the data signal to the save device, the gate connected to the first node.

As to claim 2, the modified Sani et al.'s figure 2 shows that the first latch has a second node (Q) for providing the data signal, the save device including a second transistor (Coughlin, Jr. et al.'s T11) having a gate connected to the second node.

As to claim 6, the modified Sani et al.'s figure 2 shows that the save device includes third and fourth transistors (T8, T10) respectively connected to the first and second transistors.

As to claim 7, the modified Sani et al.'s figure 2 shows that the third and fourth transistors have respective gates for receiving a control signal (FENCEN) which indicates when to transfer the data signal from the first latch to the second latch.

As to claim 9, the modified Sani et al.'s figure 2 shows that the first latch includes an inverter (260) having an input and an output, and wherein the first node is the inverter input and the second node is the inverter output.

As to claim 11, the modified Sani et al.'s figure 2 shows that the second latch is for retaining the data signal while the first latch is inoperative due to removal of power therefrom.

As to claim 13, the modified Sani et al.'s figure 2 further shows a data processing logic (circuit, not shown, that generating data signal) for performing data processing operations; plurality of resisters (the abstract teaches that the circuit having plurality of latches. The latches are interested as registers); each of the register including a plurality of data latch structures (master latch and slave latch). The combination of Sani et al. and Coughlin et al. references further shows the detail of teach data latch circuit (see the rejection of claim 1).

As to claim 14, it is seen as an intended use for using the modified Sani et al.'s circuit in a microprocessor, a microcontroller, or digital signal processor.

As to claim 15, Paragraph [0007] of Sani et al. teaches that the circuit is use in a mobile phone. Therefore, it is inherent that mobile phone having an antenna structure for permitting communication via an air interface; a wireless communication interface coupled between the antenna structure and a digital data processor (circuit, not shown, that generating data signal) for interfacing between the antenna structure and the digital data processor; and the digital data processor including a plurality of data latch structures (abstract of Sano et al.). The combination of Sani et al. and Coughlin et al. references further shows the detail of teach data latch circuit (see the rejection of claim 1).

As to claim 16, Sani et al. paragraphs [0007] teaches that circuit is use in a mobile telephone.

8. Claims 36-40 and 54-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zyuban et al. (US 20030188241) in view of Sani et al. (US 2003/0218231).

As to claims 36, 39, 54 and 56, Zyuban et al.'s figure 6B shows all limitations of the claim except for plurality of Zyuban et al.'s cirucit figure 6B are used in a wireless communication environment. However, Sani et al.'s teaches that mobile phone having plurality of registers (latches). Zyuban et al.'s latch circuit having low leakage currents. Therefore, it would have been obvious to one having ordinary skill in the art to use plurality of Zyuban et al.'s circuit figure 6B in mobile phone for the purpose of reducing leakage currents. The modified circuit further comprises a data process logic (circuit, not shown that generating data signals) for performing data process operations; an antenna structure for permitting communication via an air interface; wireless communication interface coupled between said antenna structure and said

digital data processor for interfacing between said antenna structure and said digital data processor.

As to claims 37, 55 and 57, it is seen as an intended use for using the plurality of Zyuban et al.'s circuit figure 6 in a microprocessor, microcontroller, or a digital signal processor.

As to claim 38, Zyuban et al.'s figure 6B inherently having a distribution structure (circuit, not shown, that generating signals RSTR and RSTR_b) connected to the restore devices for distributing the restore signal to the restore devices, the distribution structure power by a first power supply (Wdd), and the second latch powered by a second power supply (Vdd) other than the first power supply.

As to claim 40, plurality of Zyuban et al.'s circuit figure 6 are used in a mobile phone

Allowable Subject Matter

9. Claims 8, 10, 12, 19, 20-26, 28, 31-34, 42-47 and 50-53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8, 10, 12, 19, 28, 31-34 and 50-53 would be allowable because the prior art fails to teach or suggest first latch includes a first plurality of transistors, each transistor of the first plurality having a gate oxide, the first and/or second transistor, or the third and fourth transistors having respective gate oxides which are thicker than the gate oxides of said first plurality of transistors.

Claims 20-26 and 42-47 would be allowable because the prior art fails to teach or suggest the restore device includes a second transistor having a gate connected to the first node.

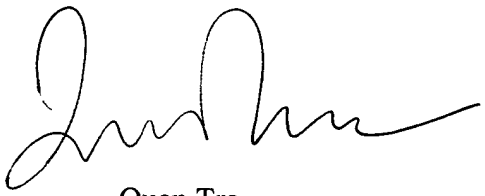
Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Quan Tra
Patent Examiner

August 17, 2004